INCH-POUND

MIL-M-38510/260
6 January 1989

MILITARY SPECIFICATION

MICROCIRCUITS, MEMORY, DIGITAL, CMOS 8K X 8 BIT, ELECTRICALLY ERASABLE, PROGRAMMABLE READ-ONLY MEMORY (EEPROM) MONOLITHIC SILICON

This specification is approved for use by all Departments and Agencies of the Department of Defense.

1. SCOPE

1.1 Scope. This specification covers the detail requirements for monolithic silicon, CMOS, 8K words/8 bit, 5.0 volts, electrically erasable programmable read-only memory microcircuits. Two product assurance classes (S and B), a choice of lead finish and three package types are provided for each device and are reflected in the complete part number.

1.2 Part or identifying number (PIN). The part or identifying number shall be in accordance with MIL-M-38510.

1.2.1 Device types. The device types shall be as shown in the following.

Device type	Circuit organization	Access time	Write speed	Write mode	End of write indicator	Endurance
01	8K words/8 bit	350 ns	10 ms	Byte/page	Data poll	10,000 cy
02	8K words/8 bit	300 ns	10 ms	Byte/page	Data poll	10,000 cy
03	8K words/8 bit	250 ns	10 ms	Byte/page	Data poll	10,000 cy
04	8K words/8 bit	200 ns	10 ms	Byte/page	Data poll	10,000 cy
05	8K words/8 bit	250 ns	10 ms	Byte/page	Data poll	100,000 cy
06	8K words/8 bit	250 ns	10 ms	Byte/page	RDY busy	10,000 cy
07	8K words/8 bit	350 ns	10 ms	Byte/page	RDY busy	10,000 cy

1.2.2 Device class. The device class shall be the product assurance level as defined in MIL-M-38510.

1.2.3 Case outlines. The case outlines shall be designated as follows:

Letter	Case outline (see MIL-M-38510, appendix C)
X	D-10 (28-lead, 1.490" x .610" x .232"), dual-in-line package
Y	C-12 (32-terminal, .560" x .458" x .120"), leadless chip carrier
Z	F-12 (28-lead, .740" x .420" x .130"), flat package

Beneficial comments (recommendations, additions, deletions) and any pertinent data which may be of use in improving this document should be addressed to: Rome Air Development Center, RBE-2, Griffiss AFB, NY 13441, by using the self-addressed Standardization Document Improvement Proposal (DD Form 1426) appearing at the end of this document or by letter.

AMSC N/A FSC 5962

1.3 Absolute maximum ratings.

All input and output voltages 1/ (including V_{CC})	-0.3 V dc to +6.0 V dc
Voltage for chip clear (V_H)	+15.0 V dc
Operating case temperature range	-55°C to +125°C
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 10 seconds)	+300°C
Thermal resistance, junction-to-case (θ_{JC})	See MIL-M-38510, appendix C
Maximum power dissipation (P_D) 2/	1.0 watt
Junction temperature (T_J) 3/	+175°C
Endurance:	
10,000 cycles/byte, minimum (Device types 01-04, 06, 07)	
100,000 cycles/byte, minimum (Device type 05)	
Data retention	10 years, minimum

1.4 Recommended operating conditions.

	Device type	Min	Max	Units
Supply voltage:				
V_{CC}	All	4.5	5.5	V dc
V_{SS}	All	0.0	0.0	V dc
High level input voltages (V_{IH})	All	2.0	V_{CC} +.3	V dc
Low level input voltages (V_{IL})	All	-0.1	0.8	V dc
Operating case temperature	All	-55	+125	°C
High level chip erase voltage (V_H)	All	12	13	V dc

2. APPLICABLE DOCUMENTS

2.1 Government documents.

2.1.1 Specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this document to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DODISS) and supplement thereto, cited in the solicitation (see 6.3).

1/ Voltages are with respect to ground. Pin voltages will be stated in this manner throughout the remainder of this specification, unless otherwise noted. Under worse case operating conditions.

2/ Under worst case operating conditions.

3/ Maximum junction temperature shall not be exceeded except for allowable short duration burn-in screening condition in accordance with method 5004 of MIL-STD-883.

SPECIFICATION

MILITARY

MIL-M-38510 - Microcircuits, General Specification for.

STANDARD

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.

(Unless otherwise indicated, copies of federal and military specifications, standards, and handbooks are available from the Naval Publications and Forms Center, (ATTN: NPODS), 5801 Tabor Avenue, Philadelphia, PA 19120-5099).

2.2 Order of precedence. In the event of a conflict between the text of this document and the references cited herein (except for related associated detail specifications, specification sheets, or MS standards), the text of this document takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Detail specifications. The individual item requirements shall be in accordance with MIL-M-38510, and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-M-38510 and herein.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Functional block diagram. The functional block diagram shall be as specified on figure 3. Upon implementing design changes, the manufacturer must submit a new block diagram to the qualifying activity for inclusion in this specification. The block diagram shall clearly define row address inputs and the column address inputs.

3.2.4 Case outlines. The case outlines shall be as specified in 1.2.3.

3.3 Lead material and finish. The lead material and finish shall be in accordance with MIL-M-38510 (see 6.5).

3.4 Electrical performance characteristics. The electrical performance characteristics are as specified in table I, and apply over the full case operating temperature range, unless otherwise specified.

3.5 Electrical test requirements. The electrical test requirements for each device class shall be the subgroups of table II. The electrical tests for each subgroup are described in table I.

3.6 Marking. Marking shall be in accordance with MIL-M-38510 and 1.2 herein. At the option of the manufacturer, the country of origin may be omitted from the body of the microcircuit but shall be retained on the initial container.

3.7 Microcircuit group assignment. The devices covered by this specification shall be in microcircuit group number 42 (see MIL-M-38510, appendix E).

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Device type	Sub-groups	Limits Min	Limits Max	Unit
Parametric characteristics 1/ 2/							
Supply current (active)	I_{CC1}	$\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = 0 mA Inputs = 5 Mhz at V_{IL} to V_{IH} V_{CC} = 5.5 V 3/	All	1,2,3		60	mA
Supply current (TTL standby)	I_{CC2}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IL}$ All I/O's = 0 mA Inputs = V_{IH}, $\overline{WE} = V_{IH}$	All	1,2,3		2	mA
Supply current (CMOS standby)	I_{CC3}	$\overline{CE} = V_{CC}$ -0.3, $\overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$ All I/O's = 0 mA Inputs = V_{IH}	All	1,2,3		250	µA
Input leakage (high)	I_{IH}	V_{CC} = 5.5 V V_{IN} = 5.5 V	All	1	-100	100	nA
				2, 3	-1	1	µA
Input leakage (low)	I_{IL}	V_{CC} = 5.5 V V_{IN} = .1 V	All	1	-100	100	nA
				2, 3	-1	1	µA
Output leakage (high)	I_{OHZ}	V_{CC} = 5.5 V V_{OUT} = 5.5 V 4/ 5/	All	1	-500	500	nA
				2, 3	-10	10	µA
Output leakage (low)	I_{OLZ}	V_{CC} = 5.5 V V_{OUT} = .1 V 4/ 5/	All	1	-500	500	nA
				2, 3	-10	10	µA
Input voltage (low)	V_{IL}	V_{CC} = 5.5 V 6/	All	1,2,3	-0.1	0.8	V
Input voltage (high)	V_{IH}	V_{CC} = 4.5 V 6/	All	1,2,3	2.0	V_{CC} +0.3	V
Output voltage (low)	V_{OL}	V_{CC}(max) = 5.5 V I_{OL} = 2.1 mA 7/	All	1,2,3		0.45	V
Output voltage (high)	V_{OH}	V_{CC}(min) = 4.5 V I_{OL} = -400 µA 8/	All	1,2,3	2.4		V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^{\circ}C \leq T_C \leq +125^{\circ}C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Device type	Sub-groups	Limits Min	Limits Max	Unit
$\overline{OE}$ high leakage (chip erase)	I_{OE}	$V_H = 13\ V$	All	1,2,3	-10	100	µA
$\overline{OE}$ high voltage	V_H	9/ 10/ 11/	All	9,10,11	12	13	V
Dynamic characteristics							
Input capacitance 2/ 12/	C_{IN}	$V_I = 0\ V$, f = 1 MHz 13/	All	4		6	pF
Output capacitance 2/ 12/	C_{OUT}	$V_O = 0\ V$, f = 1 MHz 13/	All	4		10	pF
Switching characteristics, read mode operation 2/ 14/ (see figure 4)							
Read cycle time	t_{AVAV}	9/ 10/ 15/	01,07 02 03,06 04 05	9,10,11	350 300 250 200 250		ns
Address access time	t_{AVQV}	10/ 15/	01,07 02 03,06 04 05	9,10,11		350 300 250 200 250	ns
Chip enable access time	t_{ELQV}	10/ 15/	01,07 02 03,06 04 05	9,10,11		350 300 250 200 250	ns
Output enable access time	t_{OLQV}	10/ 15/	01-02, 07	9,10,11		150	ns
			03-06			90	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Device type	Sub-groups	Limits Min	Limits Max	Unit
Chip enable to output in low Z	t_{ELQX}	10/ 12/ 15/	All	9,10,11	0		ns
Chip disable to output in high Z	t_{EHQZ}	10/ 12/ 15/ 16/	01-02, 07	9,10,11		80	ns
			03-06			60	
Output enable to output in low Z	t_{OLQX}	10/ 12/ 15/	All	9,10,11	0		ns
Output disable to output in high Z	t_{OHQZ}	10/ 12/ 15/ 16/	01-02, 07	9,10,11		80	ns
			03-06			60	
Output hold from address change	t_{AXQX}	9/ 10/ 15/	All	9,10,11	0		ns
Switching characteristics, page mode write cycle operation 9/ (see figure 4)							
Write cycle time	t_{WHWL1} t_{EHEL1}	10/ 17/	All	9,10,11		10	ms
Address setup time	t_{AVWL} t_{AVEL}	9/ 10/ 17/	All	9,10,11	20		ns
Address hold time	t_{WLAX} t_{ELAX}	9/ 10/ 17/	All	9,10,11	150		ns
Write setup time	t_{ELWL} t_{WLEL}	9/ 10/ 17/	All	9,10,11	0		ns
Write hold time	t_{WHEH} t_{EHWH}	9/ 10/ 17/	All	9,10,11	0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Device type	Sub-groups	Limits		Unit
					Min	Max	
Output enable setup time	t_{OHWL} t_{OHEL}	9/ 10/ 17/	All	9,10,11	20		ns
Output enable hold time	t_{WHOL} t_{EHOL}	9/ 10/ 17/	All	9,10,11	20		ns
Write pulse width	t_{WLWH} t_{ELEH}	9/ 10/ 17/	All	9,10,11	150		ns
Data setup time	t_{DVWH} t_{DVEH}	9/ 10/ 17/	All	9,10,11	50		ns
Data hold time	t_{WHDX} t_{EHDX}	9/ 10/ 11/	All	9,10,11	10		ns
Byte load cycle	t_{WHWL2} t_{EHEL2}	9/ 10/ 18/	All	9,10,11	.2	200	µs
Last byte loaded to data polling	t_{WHEL} t_{EHEL}	9/ 10/ 17/	All	9,10,11		200	µs
Delay to next write	t_{DVWL} t_{DVEL}	9/ 10/ 16/ 17/	All	9,10,11		10	µs
Switching characteristics, chip erase mode operation (see figure 4)							
$\overline{CE}$ setup time	t_{ELWL}	9/ 10/ 11/	All	9,10,11	1		µs
$\overline{OE}$ setup time	t_{OVHWL}	9/ 10/ 11/	All	9,10,11	1		µs
$\overline{WE}$ pulse width	t_{WLWH2}	9/ 10/ 11/	All	9,10,11	150		ns
$\overline{CE}$ hold time	t_{WHEH}	9/ 10/ 11/	All	9,10,11	1		µs

See footnotes on next page.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions $-55^\circ C \leq T_C \leq +125^\circ C$ $4.5\ V \leq V_{CC} \leq 5.5\ V$ unless otherwise specified	Device type	Sub-groups	Limits		Unit
					Min	Max	
$\overline{OE}$ hold time	t_{WHOH}	9/ 10/ 11/	All	9,10,11	1		µs
Erase time	t_{OHEL}	9/ 10/ 11/	All	9,10,11		200	ms
High voltage	V_H	9/ 10/ 11/	All	9,10,11	12	13	V

1/ DC and read mode.

2/ All pins not being tested are to be open.

3/ The test in subgroups 1, 2, and 3 toggles addresses at 5 MHz during measurements of I_{CC} active. Test performed with outputs unloaded.

4/ Terminal conditions for the output leakage current test shall be as follows:

a. V_{IH} = 2.0 V; V_{IL} = 0.8 V.

b. For I_{OLZ}: Select an appropriate address to acquire a logic "1" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

c. For I_{OHZ}: Select an appropriate address to acquire a logic "0" on the designated output. Apply V_{IH} to $\overline{CE}$. Measure the leakage current while applying the specified voltage.

5/ Connect all address inputs and $\overline{OE}$ to V_{IH} and measure I_{OLZ} and I_{OHZ} with the output under test connected to V_{OUT}.

6/ A functional test shall verify the dc input and output levels and applicable patterns as appropriate. All address locations shall be tested. Terminal conditions are as follows:

a. Inputs: H = 2.0 V; L = 0.8 V.

b. Outputs: H = 2.4 V minimum and L = 0.4 V maximum.

c. The functional tests shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

7/ An input preconditioning logic sequence shall be applied that results in a logic "0" at the output to be measured. Logic input levels are V_{IL} = 0.8 V and V_{IH} = 2.0 V.

8/ An input preconditioning logic sequence shall be applied that results in a logic "1" at the output to be measured. Logic input levels are V_{IL} = 0.8 V and V_{IH} = 2.0 V.

9/ Tested by application of specified timing signals and conditions.

10/ The outputs are loaded in accordance with figure 5 (or equivalent).

11/ These tests in subgroups 9, 10, and 11 are the chip erase cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8, by application of the timing limits and signal levels in table I. Timing diagrams appear on figure 4. Subgroups 7, 8, 9, 10, and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

12/ Only performed for initial qualification and after any design or process change that could affect that parameter.

13/ Input/output capacitance shall be measured between the designated terminal and the GND pin under the following conditions: V_I = 0 V, f = 1 MHz, oscillator voltage = 50 mV rms maximum. Unused pins are open.

14/ Equivalent ac test conditions:

Output load: 1 TTL gate and C_L = 100 pF
Input rise and fall times $\leq$ 10 ns
Input pulse levels: 0.4 V and 2.4 V
Timing measurement reference levels:
Inputs 1 V and 2 V
Outputs 0.8 V and 2 V

15/ Timing diagrams appear on figure 4. Subgroups 9, 10, and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. The manufacture shall define a worse addressing algorithm, e.g., column galpat diagonal incrementing, address complement, that shall be approved by the qualifying activity.

16/ Tested by inference only.

17/ These tests in subgroups 9, 10, and 11 are the byte write cycle limits. These parameters shall be verified during functional testing, subgroups 7 and 8 by application of the timing limits in table I. Timing diagrams appear on figure 4. Subgroups 7, 8, 9, 10, and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ and $\overline{CE}$ (e.g., for $\overline{WE}$ and $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

18/ These tests in subgroups 9, 10, and 11 are the page mode write cycle limits. These parameters shall be verified during the functional testing, subgroups 7 and 8 by application of the timing limits in table I. Timing diagrams appear on figure 4 subgroups 7, 8, 9, 10, and 11 shall be performed with V_{CC} = 4.5 V and V_{CC} = 5.5 V.

TABLE II. Electrical test requirements. 1/ 2/ 3/

MIL-STD-883 test requirements	Subgroups (see table III)	
	Class S devices	Class B devices
Interim electrical parameters (method 5004)	1,7,9, or 2,8(+125°C),10	1, 7, 9, or 2,8,(+125°C),10
Final electrical test parameters (method 5004)	1*,2,3,7*,8, 9,10,11	1*,2,3,7*,8, 9,10,11
Group A test requirements (method 5005)	1,2,3,4**,7, 8,9,10,11	1,2,3,4**,7, 8,9,10,11
Group B test requirements (method 5005, subgroup 5)	1,2,3,7,8, 9,10,11	Not applicable
Group C end-point electrical parameters (method 5005)	Not applicable	1,2,3,7,8, 9,10,11 4/
Group D end-point electrical parameters (method 5005)	1,2,3,7,8, 9,10,11	1,2,3,7,8, 9,10,11

* The PDA applies to subgroups 1 and 7 (see 4.2c).

** Subgroup 4 (capacitance) is measured only upon initial qualification and for redesign (see 4.4.1c).

1/ For all electrical tests, the device shall be programmed to the data pattern specified.

2/ Any or all subgroups at the same temperature may be combined when using a multifunction tester.

3/ Subgroups 7 and 8 shall consist of writing and reading the data patterns specified in accordance with the limits of table I, subgroups 9, 10, and 11.

4/ Delta limits shall be required on initial qualification or after any major design change. Delta values shall be computed with reference to the previous interim electrical parameters (see 4.4.3).

3.8 Processing of EEPROMs. All testing requirements and quality assurance provisions herein shall be satisfied by the manufacturer prior to delivery.

3.8.1 Conditions of the supplied devices. Devices will be supplied in an unprogrammed or cleared state. No provision will be made for supplying programmed devices.

3.8.2 Erasure of EEPROMs. When specified, devices shall be erased in accordance with the procedures and characteristics specified in 4.5.4.

3.8.3 Programming of EEPROMs. When specified, devices shall be programmed in accordance with the procedures and characteristics specified in 4.5.3.

3.8.4 Verification of state of EEPROMs. When specified, devices shall be verified as either programmed to the specified pattern or erased. As a minimum, verification shall consist of performing a read of the entire array to verify that all bits are in the proper state. Any bit that does not verify to be in the proper state shall constitute a device failure, and the device shall be removed from the lot or sample.

3.8.5 Power supply sequence of EEPROMs. In order to reduce the probability of inadvertent writes, the following power supply sequences shall be observed:

a. A logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the application of V_{CC}.

b. A logic high state shall be applied to $\overline{WE}$ and/or $\overline{CE}$ at the same time or before the removal of V_{CC}.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Inspection procedures shall be in accordance with MIL-M-38510 and method 5005 of MIL-STD-883, except as modified herein.

4.2 Screening. Screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to qualification and quality conformance inspection. The following additional criteria shall apply.

a. Burn-in test (method 1015) of MIL-STD-883):

(1) Test condition D or F using the circuits shown on figure 6 or equivalent.

(2) $T_A = +125°C$, minimum.

(3) Prior to burn-in, the devices shall be programmed (see 3.8.3) with the data pattern shown on figure 7. The pattern shall be read before and after burn-in. Devices having bits not in the proper state after burn-in shall constitute a device failure and shall be included in the PDA calculation (see 4.2c).

b. Interim and final electrical test parameters shall be as specified in table II. Interim electrical test parameters prior to burn-in must be performed by the manufacturer. The following data patterns shall be included in group A subgroups 7 or 8 (high and low temperature). All 0's, all 1's, checkerboard and checkerboard complement. Each temperature shall include, at a minimum, the programming of one data pattern. Subgroups 9, 10, and 11 shall be performed on devices containing a checkerboard and a checkerboard complement data patterns or equivalent alternating bit and complementary data patterns.

c. Percent defective allowable (PDA): The PDA for class B devices shall be as specified in MIL-M-38510. The PDA is specified as 5 percent for class B devices based on failures from group A, subgroups 1 and 7 after cooldown, at final electrical test in accordance with method 5004 of MIL-STD-883, and with no intervening electrical measurements. All screening failures of group A, subgroups 1 and 7 after burn-in divided by the total number of devices submitted to burn-in in that lot shall be used to determine the percent defective for that lot, and the lot shall be accepted or rejected based on the PDA.

d. Those devices whose measured characteristics, after burn-in, exceed the specified delta (Δ) limits or electrical parameter limits specified in table I, subgroup 1, are defective and shall be removed from the lot. The verified failures divided by the total number of devices in the lot initially submitted to burn-in shall be used to determine the percent defective for the lot and the lot shall be accepted or rejected based on the specified PDA.

e. An endurance test including a data retention bake, in accordance with method 1033 of MIL-STD-883, prior to burn-in (e.g., may be performed at wafer sort) shall be included as part of the screening procedure, with the following conditions:

(1) Cycling may be block, byte, or page at equipment room ambient temperature and shall cycle all bytes for a minimum of 10,000 cycles for device types 01-04, 06, 07, and a minimum of 50,000 cycles for device type 05.

(2) After cycling, perform a high temperature unbiased bake for 72 hours at +150°C (minimum). The storage time may be accelerated by using higher temperature in accordance with the Arrhenius relationship:

$$A_F = e^{-\frac{E_A}{K}\left[\frac{1}{T_1} - \frac{1}{T_2}\right]}$$

A_F = acceleration factor (unitless quantity) = t_1/t_2

T = temperature in Kelvin (i.e., t_1 + 273)

t_1 = time (hours) at temperature T_1.

t_2 = time (hours) at temperature T_2.

K = Boltzmanns constant = 8.62×10^{-5} eV/°K using an apparent activation energy (E_A) of 0.6 volt.

The maximum storage temperature shall not exceed +200°C for packaged devices or +300°C for unassembled devices. All devices shall be programmed with a charge opposite the state that the cell would read in its equilibrium state (e.g., worst case pattern).

(3) Read the data retention pattern and test using subgroups 1, 7, and 9 (at the manufacturer's option, high temperature equivalent subgroups 2, 8, and 10 or low temperature equivalent subgroups 3, 8, and 11 may be used in lieu of subgroups 1, 7, and 9) after cycling and bake, prior to burn-in. Devices having bits not in the proper state after storage shall constitute a device failure.

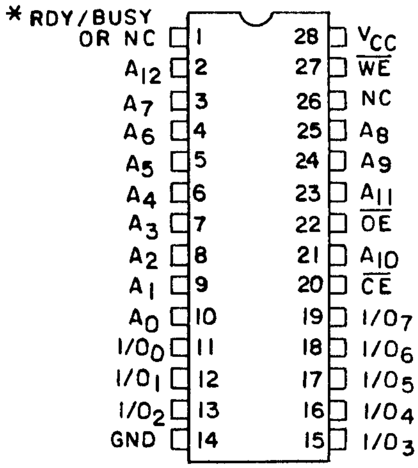
f. After the completion of all screening, the devices shall be erased and verified prior to delivery.

4.3 Qualification inspection. Qualification inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspections (see 4.4.1 through 4.4.4).

4.3.1 Qualification extension. When authorized by the qualifying activity, for qualification inspection, if a manufacturer qualifies to a faster device type which is manufactured identically to a slower device type on this specification, the slower device type may be part I qualified without further qualification testing. At the manufacturer's request, the slower device types will be added to the QPL.

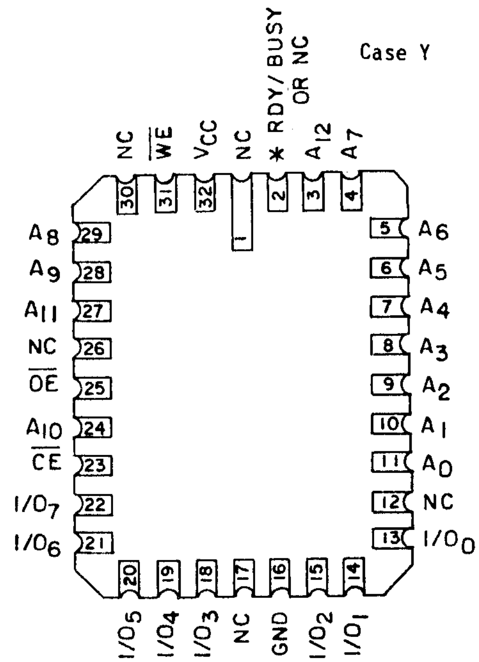
All device types
top view

Case X



All device types
bottom view

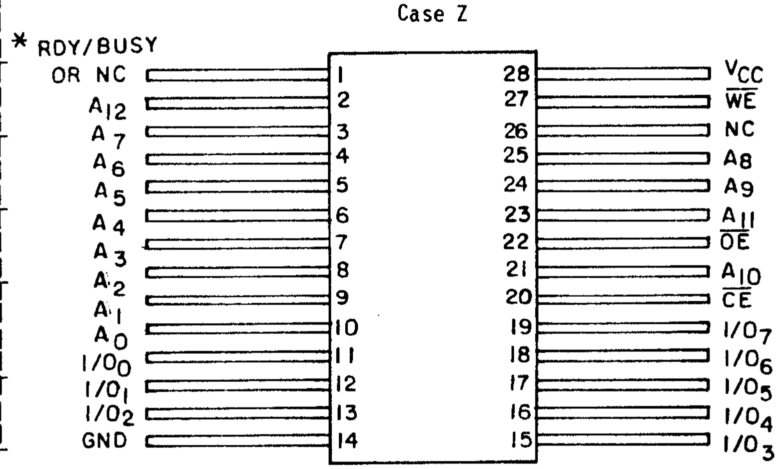
Case Y



All device types

A_0-A_5	Addresses-column
A_6-A_{12}	Addresses-row
$\overline{CE}$	Chip enable
$\overline{OE}$	Output enable
$\overline{WE}$	Write enable
I/O 0-7	Data input (write) data output (read)
NC	No connection

Case Z



* NC for device types 01-05, RDY/BUSY for device types 06 and 07.

FIGURE 1. Terminal connections.

Mode	Inputs			I/O	Ready busy	Device type
	$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	I/O 0 - I/O 7		
Read	V_{IL}	V_{IL}	V_{IH}	D_{OUT}	High Z	All
Write	V_{IL}	V_{IH}	V_{IL}	D_{IN}	V_{OL}	All
Standby	V_{IH}	X	X	High Z	High Z	All
Write inhibit	X	V_{IL}	X	X	High Z	All
Write inhibit	X	X	V_{IH}	X	High Z	All
Chip erase	V_{IL}	V_H	V_{IL}	X	High Z	All
Data polling	V_{IL}	V_{IL}	V_{IH}	All I/O or I/07	High Z	All

Table definitions:

V_{IH} = High logic level
V_{IL} = Low logic level
V_H = Chip clear voltage (15)
X = Do not care

High Z = High impedance state
D_{IN} = Data input
D_{OUT} = Data output

FIGURE 2. Truth table for unprogrammed devices.

All device types

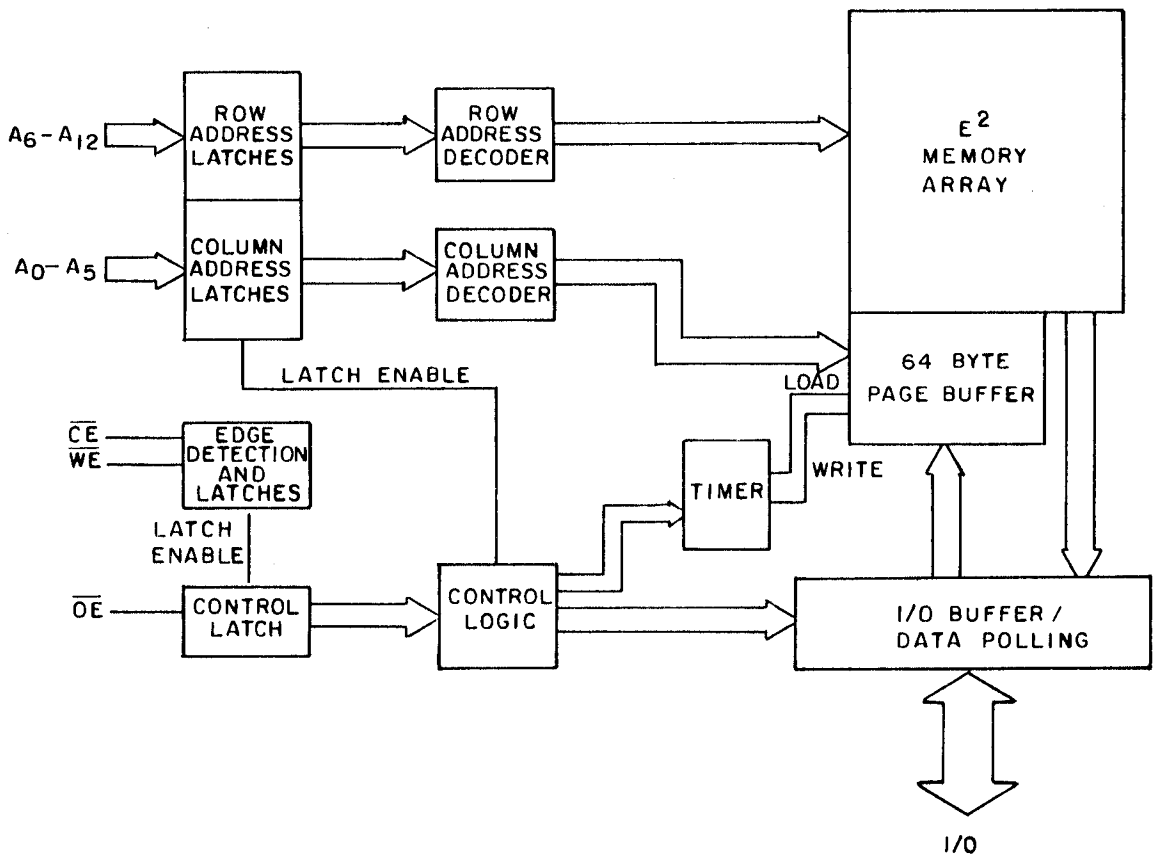
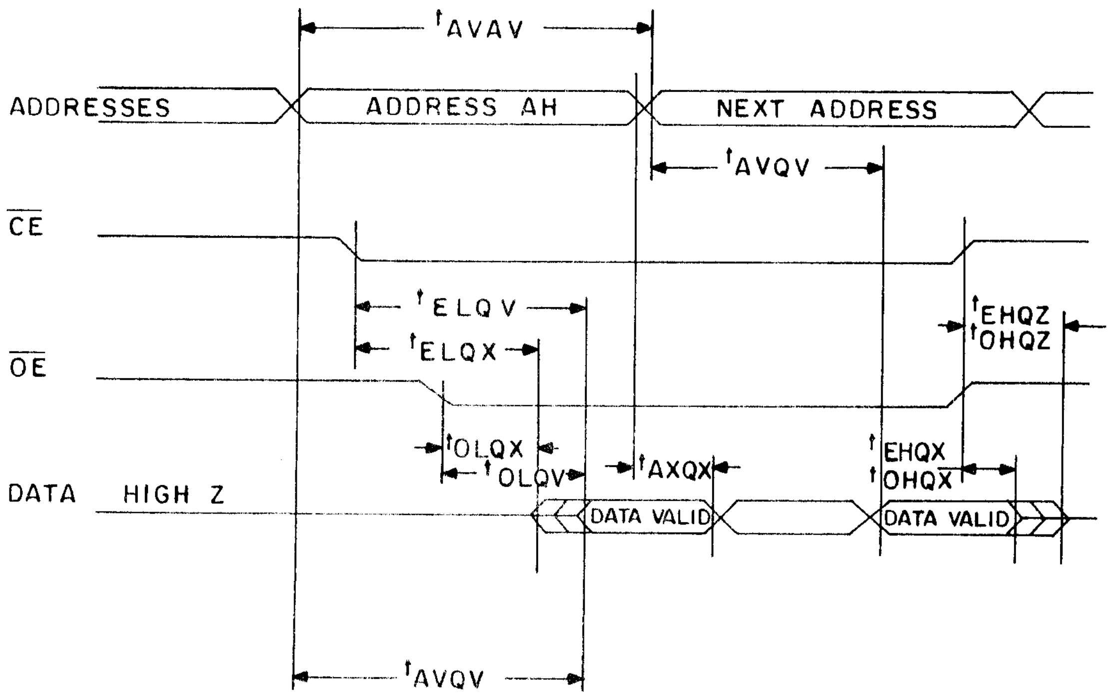


FIGURE 3. Functional block diagram.

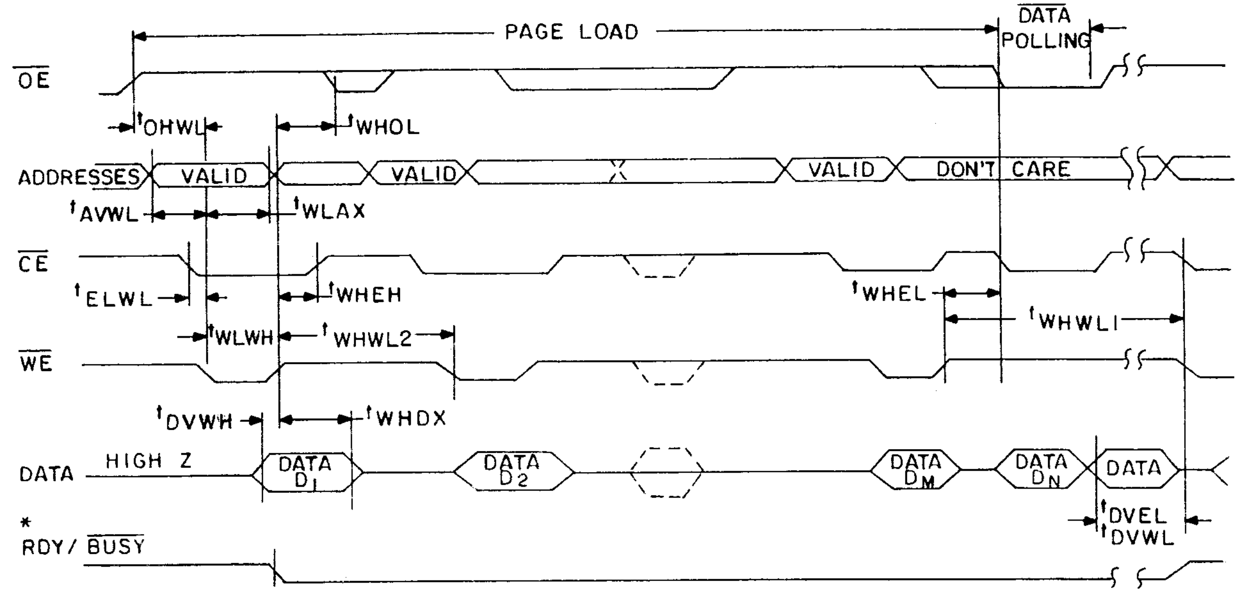


Read mode

NOTES:
1. V_{CC} shall be applied simultaneously or after $\overline{WE}$ and removed simultaneously or before $\overline{WE}$.
2. Output load is a TTL gate and 100 pF including jig or probe capacitance.
3. Input rise and fall time $\leq$ 20 ns.
4. Input pulse levels of 0.4 V and 2.4 V.
5. Timing measurement reference levels:
   Inputs 1.0 V and 2.0 V.
   Outputs 0.8 V and 2.0 V.

FIGURE 4. Timing waveforms.

All device types

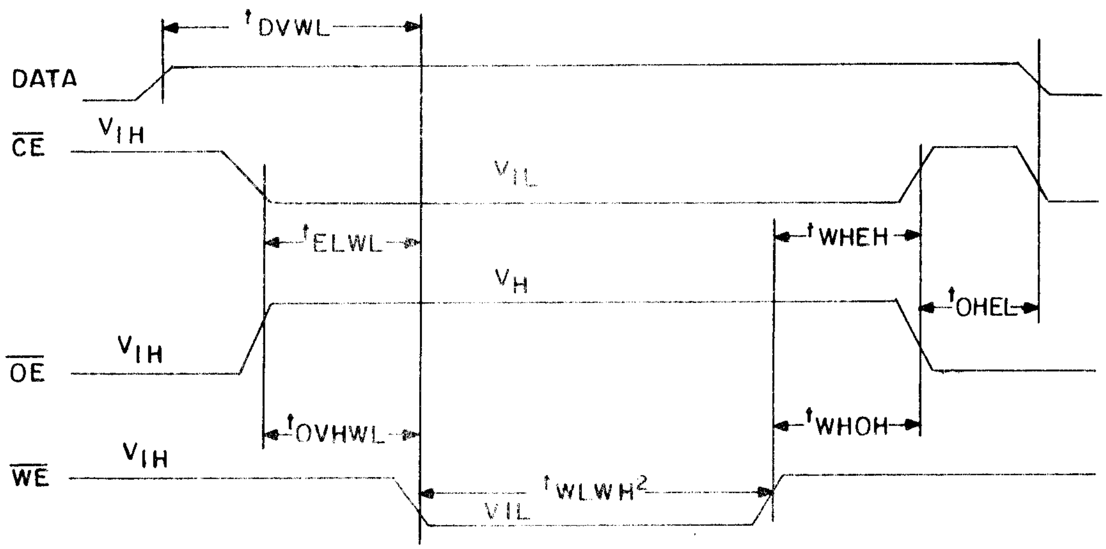


Page mode write cycle

NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10 percent and 90 percent) $\leq$ 20 ns.
4. Input pulse levels are 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. Page load is 1 to 64 bytes of data.
7. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
8. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.
9. Page write cycle timings are referenced to the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is last to go low, and the $\overline{WE}$ or $\overline{CE}$ inputs, whichever is first to go high.
10. Bytes may be loaded and re-loaded at random within a page load cycle. The page addresses must remain the same for each successive write operation throughout the page load cycle. Between successive byte writes within a page write operation, $\overline{OE}$ can be strobed low; e.g., this can be done for the next write; or with $\overline{WE}$ high and $\overline{CE}$ low effectively performing a polling operation.

FIGURE 4. Timing waveforms - Continued.

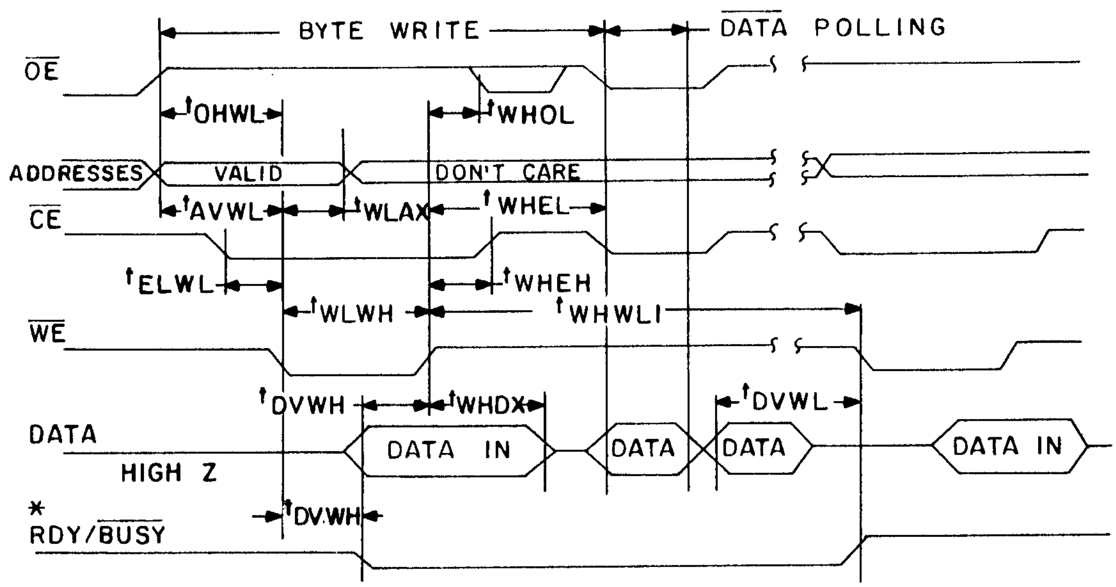
All device types



Chip erase mode

FIGURE 4. Timing waveforms - Continued.

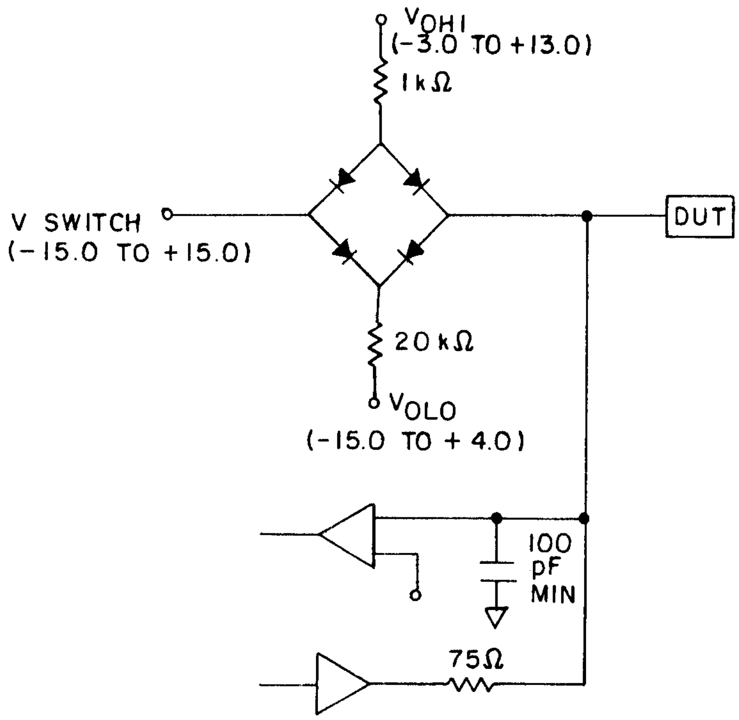
All device types



Byte write mode ($\overline{WE}$ and $\overline{CE}$ controlled)

NOTES:
1. Input timing reference levels are 1.0 V and 2.0 V.
2. Output timing reference levels are 0.8 V and 2.0 V.
3. Input pulse rise and fall times (10 percent and 90 percent) ≤ 20 ns.
4. Input pulse levels are 0.4 V and 2.4 V.
5. Program verify equivalent to the read mode.
6. $\overline{WE}$ is noise protected. Less than a 20 ns write pulse will not activate a write cycle.
7. $\overline{WE}$ and $\overline{CE}$ both must be active to initiate a write cycle; therefore, the sequence of $\overline{WE}$ or $\overline{CE}$ (e.g., for $\overline{WE}$ or $\overline{CE}$ controlled write) is verified interchangeable without duplicate testing.

FIGURE 4. Timing waveforms - Continued.

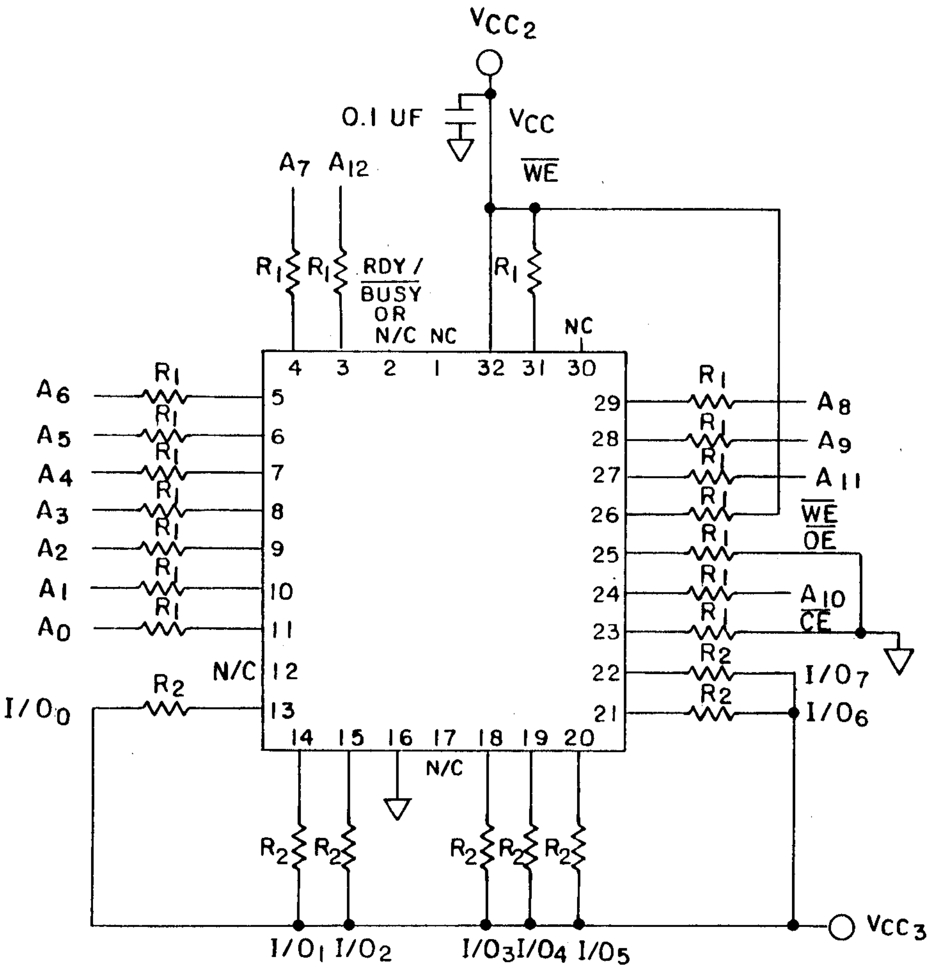


NOTE: V_{OHI} and V_{OLO} will be adjusted to meet load conditions of table I.

FIGURE 5. Switching load circuit.

Case Y (LCC)

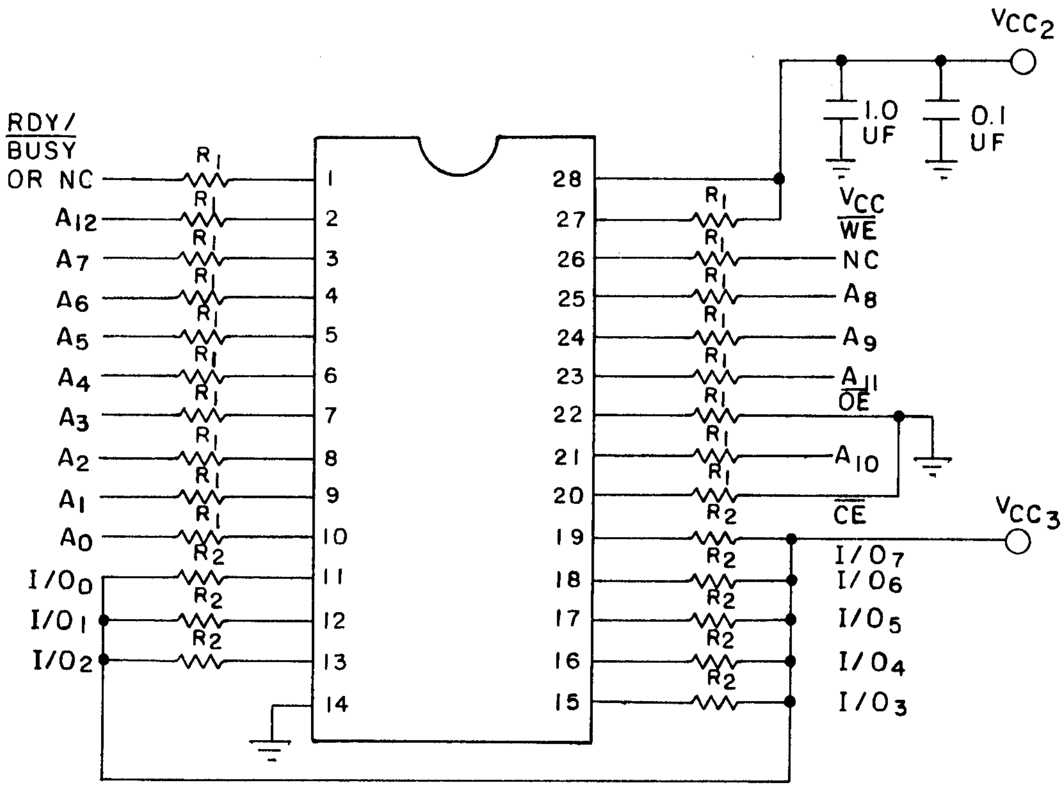
All device types



NOTES:
1. All resistors labeled R_1 are 3.3 kΩ, 1/4 W, 5 percent carbon film at every socket.
2. All resistors labeled R_2 are 2.2 kΩ, 1/4 W, 5 percent carbon film at every socket.
3. There is a 0.1 uF decoupling capacitor between V_{CC} and GND, at every socket.
4. $V_{CC1} = V_{CC2} = 5.25$ V, $V_{CC3} = 2.5$ V, all voltage levels are ±0.25 V.
5. Power up sequence: V_{CC1}, V_{CC2}, addresses, V_{CC3}.
6. Power down sequence: V_{CC3}, addresses, V_{CC2}, V_{CC1}.
7. Resistor at pin 2 can be 200Ω as an alternative.
8. F_0 (A_0) = 500 kHz.
9. F_1 (A_1) = F_0 divided by 2, F_2 (A_2) = F_1 divided by 2 ...F_{12} (A_{12}) = F_{11} divided by 2.

FIGURE 6. Burn-in and operating life test circuit.

Case X (CERDIP) Case Z (flat pack) all device types



NOTES:
1. All resistors labeled R_1 are 3.3 kΩ, 1/4 W, 5 percent metal film at every socket.
2. All resistors labeled R_2 are 2.3 kΩ, 1/4 W, 5 percent metal film at every socket.
3. There is a 0.1 uF decoupling capacitor between pins 1/27 and GND, at every socket.
4. There is a 0.1 µF decoupling capacitor between V_{CC} and GND at every socket.
5. $V_{CC1} = V_{CC2} = 5.25$ V, $V_{CC3} = 2.25$ V. All voltage levels are ±0.25 V.
6. Power up sequence: V_{CC1}, V_{CC2}, addresses, V_{CC3}.
7. Power down sequence: V_{CC3}, addresses, V_{CC2}, V_{CC1}.
8. F_0 (A_0) = 500 kHz.
9. F_1 (A_1) = F_0 divided by 2, F_2 = F_1 divided by 2 ... F_{12} (A_{12}) = F_{11} divided by 2.

FIGURE 6. Burn-in and operating life test circuit - Continued.

Column address (see notes)

		0	1	2	3	4	5	6		25	26	27	28	29	30	31
	0	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	1	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
	2	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	3	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
R	.								. . .							
O	.								. . .							
W	.								. . .							
	124	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
A	125	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
D	126	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
D	127	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
R	.								. . .							
R	.								. . .							
E	.								. . .							
S	.								. . .							
S	252	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
	253	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55
See note 1																
	254	AA	AA	AA	AA	AA	AA	AA	. . .	AA	AA	AA	AA	AA	AA	AA
See note 2																
	255	55	55	55	55	55	55	55	. . .	55	55	55	55	55	55	55

NOTES:
1. All address numbers shown in decimal.
2. Each column/row address location corresponds to 1 byte.
3. All data numbers shown in hexadecimal.
   AA = 10101010 55 = 01010101
4. Manufacturers at their option may employ an equivalent pattern provided it is a topologically true alternating bit pattern.

FIGURE 7. Data pattern.

4.3.2 Electrostatic discharge sensitivity qualification inspection. Electrostatic discharge sensitivity (ESDS) testing shall be performed in accordance with MIL-STD-883, method 3015. The option to categorize devices as ESD sensitive without performing the test is not allowed. Only those device types that pass ESDS testing at 1,000 volts or greater shall be considered as conforming to the requirements of this specification. ESDS testing shall be measured only for initial qualification and after process or design changes which may affect ESDS classification.

4.4 Quality conformance inspection. Quality conformance inspection shall be in accordance with MIL-M-38510. Inspections to be performed shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, and D inspection (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection. Group A inspection shall be in accordance with table I of method 5005 of MIL-STD-883 and as follows:

a. Electrical test requirements shall be as specified in table II herein.

b. Subgroups 5 and 6 of table I of method 5005 of MIL-STD-883 shall be omitted.

c. Subgroup 4 (C_{IN} and C_{OUT} measurements) shall be measured for initial qualification and after process or design changes which affect capacitance. Sample size is 15 devices, all input and output terminals, with an accept on zero.

4.4.2 Group B inspection. Group B inspection shall be in accordance with table II of method 5005 of MIL-STD-883. All class S devices selected for testing shall be programmed (see 3.8.3) with pattern shown on figure 7.

4.4.3 Group C inspection. Group C inspection shall be in accordance with table III of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. All devices requiring end-point electrical testing shall be programmed with the pattern shown on figure 7.

c. Steady-state life test (method 1005 of MIL-STD-883) conditions:

(1) Test condition D or F as specified in 4.5.2 and figure 6 (or equivalent).

(2) Ambient temperature equals +125°C minimum.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

(4) Read the pattern after burn-in and perform end-point electrical tests in accordance with table II herein for group C.

(5) Delta measurements: Delta measurements, as specified in table II, shall be made and recorded before and after the required burn-in screens and steady-state life tests to determine delta compliance. The electrical parameters to be measured with associated delta limits are listed in table III.

TABLE III. Delta limits at +25°C.

Parameters	Limits 1/
I_{CC3}	±10 percent of specified limit
I_{IH}	±10 percent of specified limit
I_{IL}	±10 percent of specified limit
I_{OHZ}	±10 percent of specified limit
I_{OLZ}	±10 percent of specified limit
I_{OE}	±10 percent of specified limit

1/ Delta limits apply to an increase or decrease from the initial value (e.g., pre-life test I_{IH} = -120 nA, post-life test I_{IH} = -170 nA).

d. An endurance test, in accordance with method 1033 of MIL-STD-883, shall be added to group C, subgroup 1 inspection prior to performing the steady-state life test (see 4.4.3c) and extended data retention (see 4.4.3e). Cycling may be block, byte, or page from devices passing group A after the completion of the requirements of 4.2 herein. Initially two groups of devices shall be formed, cell 1 and cell 2. The following conditions shall be met:

(1) Cell 1 shall be cycled at -55°C and cell 2 shall by cycled at +125°C for a minimum of 10,000 cycles for device types 01-04, 06, 07; 100,000 cycles for device type 05 (see 1.2.1) per device type.

(2) Perform group A, subgroups 1, 7, and 9 after cycling. Form new cells (cell 3 and cell 4) for steady-state life and extended data retention. Cell 3 for steady-state life test consists of one-half of the devices from cell 1 and one-half of the devices from cell 2. Cell 4 for extended data retention consists of the remaining devices from cell 1 and cell 2.

(3) The sample plans for cell 1, cell 2, cell 3, and cell 4 shall individually be the same as for group C, subgroup 1, as specified in method 5005 of MIL-STD-883.

e. Extended data retention shall consist of the following:

(1) Program all bits in each device with the data pattern representing the worst case data retention pattern (see 4.2.d(2)).

(2) After cycling, preform a high temperature unbiased bake for 72 hours at +150°C minimum. The bake time may be accelerated by using a higher temperature in accordance with the Arrhenius relationship and with the apparent activation energy of .6 eV. The maximum bake temperature shall not exceed +175°C.

(3) Read the pattern after bake and perform end-point electrical tests for table II herein for group C.

f. Cell 1, cell 2, cell 3, and cell 4 must individually pass the specified sample plan.

4.4.4 Group D inspection. Group D inspection shall be in accordance with table IV of method 5005 of MIL-STD-883 and as follows:

a. End-point electrical tests shall be as specified in table II herein.

b. All devices selected for electrical testing shall be programmed with the pattern shown on figure 7. After completion of all testing, the devices shall have the programmed pattern read, then be erased and verified. When the use of electrical rejects is permitted, no programming, erasure, or verification is required.

4.5 Methods of inspection. Method of inspection shall be as specified in the appropriate tables and as follows.

4.5.1 Voltages and current. All voltages given are referenced to the microcircuit ground terminal. Currents given are conventional and positive when flowing into the referenced terminal.

4.5.2 Life test, burn-in, cooldown, and electrical test procedure. When devices are measured at +25°C following application of the steady-state life or burn-in test condition, all devices shall be cooled to +35°C or within +10°C of power stable condition prior to removal of bias within +10°C of power stable condition prior to removal of bias voltages/signals. Any electrical tests required shall first be performed at -55°C or +25°C prior to any required tests at +125°C.

4.5.3 Programming procedure. The waveforms and timing relationships shown on figure 4 and the conditions specified in table I shall be adherred to. Initially and after each chip erasure (see 4.5.4), all bits are in the high state (output at V_{OH}).

4.5.3.1 Byte write operation. Information is introduced by selectively programming (logic 0 level) or H (logic 1 level) into the desired bit locations. A programmed L can be changed to an H by programming an H. No erasure is necessary (see 4.5.4).

4.5.3.2 Page write operation. The page write operation can be initiated during any write operation. Following the initial byte write cycle, the host can write an additional 1 to 63 bytes in the same manner as the first byte was written. Each successive byte load cycle, started by the $\overline{WE}$ ($\overline{CE}$) high to low transition, must begin within 150 µs of the falling edge of the preceding $\overline{WE}$ ($\overline{CE}$) high to low transition, $t_{WLWH1}+t_{WHWHL2}$ or $t_{ELEH1}+t_{ELEH2}$. If a subsequent $\overline{WE}$ high to low transition is not detected within 150 ms, the internal automatic programming cycle will commence. The successive writes need not be sequential; however, the page address (A_6 through A_{12}) for each write during a page write operation shall be the same.

4.5.3.3 Data polling operation. During the internal programming cycle after a byte or page write operation, an attempt to read the last byte written will produce the complement of that data on all I/0 or I/07 (i.e., write data, 0XXX XXXX and read data, 1XXX XXX). Once the programming cycle has completed, all I/0 or I/07 will reflect true data (i.e, write data, 0XXX XXX read data, 0XXX XXX).

4.5.4 Erasing procedure. The waveforms and timing relationship shown on figure 4 and the conditions specified in table I shall be adherred to. Initially and after each chip erasure, all bits are in the high state (output at V_{OH}).

4.5.4.1 Byte erasure. A byte is erased by simultaneously programming a high state into each bit at the selected address (see 4.5.3). This can be done via a byte write cycle or a page mode write cycle (see figure 4).

4.5.4.2 Chip erase. The device is erased by setting the $\overline{OE}$ output enable pin to high state (see figure 4), while all other inputs are set in the normal byte erase mode (see 4.5.4.1). After chip erasure, all bits are in the high state. (Applies to all device types).

4.5.5 Read mode operation. The device is in the read mode whenever the $\overline{CE}$ and $\overline{OE}$ pins are at V_{IL} and the $\overline{WE}$ pin is at V_{IH}. The waveforms and timing relationship shown on figure 4 and the test conditions and limits specified in table I shall be applied.

4.5.6 Extended page load. Device types 01-06 page mode's faster average byte write time, data must be loaded at the page load cycle time (tBLC). The write cycle must "stretched" by maintaining $\overline{WE}$ low, assuming a write enable-controlled cycle, and leaving all other control inputs ($\overline{CE}$, $\overline{OE}$) in the proper page load cycle state. Since the page load timer is reset on the falling edge of $\overline{WE}$, keeping this signal low will inhibit the page timer. When $\overline{WE}$ returns high, the input data is latched and the page load cycle timer begins in $\overline{CE}$ controlled write the same is true, with $\overline{CE}$ holding the timer reset instead of $\overline{WE}$.

4.5.7 RDY/$\overline{BUSY}$. While the write operation is in progress, the RDY/$\overline{BUSY}$ output is at a TTL low. An internal timer times out the required byte write time and at the end of this time, the device signals the RDY/$\overline{BUSY}$ pin to a TTL high. The RDY/$\overline{BUSY}$ pin is an open drain output and a typical 3 kΩ pull-up resistor to V_{CC} is required. The pull-up resistor value is dependent on the number of OR-tied RDY/$\overline{BUSY}$ pins (applies to device types 06 and 07).

4.6 Inspection of packaging. The sampling and inspection of the preservation, packing, and container marking shall be in accordance with the requirements of MIL-M-38510.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-M-38510. The devices covered by this specification require electrostatic protection.

6. NOTES

(This section contains information of a general or explanatory nature that may be helpful, but is not mandatory.)

6.1 Notes. The notes specified in MIL-M-35810 are applicable to this specification.

6.2 Intended use. Microcircuits conforming to this specification are intended for original equipment design applications and logistic support of existing equipment.

6.3 Ordering data. The contract or purchase order should specify the following:

a. Complete part or identifying number (see 1.2).

b. Requirements for delivery of one copy of the quality conformance inspection data pertinent to the device inspection lot to be supplied with each shipment by the device manufacturer, is applicable.

c. Requirements for certificate of compliance, if applicable.

d. Requirements for notification of change of product or process to the contracting activity in addition to notification to the qualifying activity, if applicable.

e. Requirements for failure analysis (including required test condition of MIL-STD-883, method 5003), corrective action and reporting of results, if applicable.

f. Requirements for product assurance options.

g. Requirements for special lead lengths or lead forming if applicable. These requirements shall not affect the part number. Unless otherwise specified, these requiements shall not apply to direct purchase or direct shipment to the Government.

h. Requirements for JAN marking.

6.4 Abbreviations, symbols and definitions. The abbreviations, symbols, and definitions used herein defined in MIL-M-38510, MIL-STD-1331 (including terms and symbols for device terminals) and as follows:

V_{SS}	-	Common or reference voltage mode.
V_{CC}	-	Supply voltage.
V_H	-	Output enable and write enable voltage during chip erase.
A_0-A_{12}	-	Address inputs used to address 1 of 2048/8 bit locations in static storage array.
$\overline{CE}$	-	Chip enable used with the output enable ($\overline{OE}$) signal to control the state of the 8 data I/O signals.
$\overline{OE}$	-	Output enable used to control the I/O terminals.
DQ_0-DQ_7	-	Data I/O, 8 bit wide data bus.
$\overline{WE}$	-	Write enable input used to select a write mode.
I_{CC1}	-	Supply current (standby and active).
I_{CC2}	-	Supply current (TTL standby).
I_{CC3}	-	Supply current (CMOS standby).
I_{oe}	-	Output enable high voltage current.
I_{IH},I_{IL}	-	Input leakage currents.
I_{OHZ},I_{OLZ}	-	High impedance output leakage current.
V_{IL}	-	Logical low input voltage.
V_{IH}	-	Logical high input voltage.
V_{OL}	-	Logical low output voltage.
V_{OH}	-	Logical high output voltage.
C_{IN}	-	Input capacitance.
C_{OUT}	-	Output capacitance.
t_{AVAV}	-	Cycle time from one read to next read.

t_{ELQV} - Chip enable access time.

t_{AVQV} - Address access time.

t_{OLQV} - Output enable access time.

t_{ELQX} - Chip enable to output in low Z.

t_{EHQZ} - Chip enable to output in high Z.

t_{OLOZ} - Output enable to output in low Z.

t_{OHQZ} - Output enable to output in high Z.

t_{AXQX} - Output hold from address change.

t_{WHWL1} - Cycle time during $\overline{WE}$ write operation.

t_{EHEL1} - Cycle time during $\overline{CE}$ write operation.

t_{AVWL} - Address to $\overline{WE}$ setup time.

t_{AVEL} - Address to $\overline{CE}$ setup time.

t_{WLAX} - Address hold time after $\overline{WE}$ low.

t_{ELAX} - Address hold time after $\overline{CE}$ low.

t_{ELWL} - Chip enable to $\overline{WE}$ setup time.

t_{WLEL} - Write enable to $\overline{CE}$ setup time.

t_{WHEH} - Chip enable hold time after $\overline{WE}$ high.

t_{EHWH} - Write enable hold time after $\overline{CE}$ high.

t_{ELEH} - Chip enable pulse width during write.

t_{OHWL} - Output enable to $\overline{WE}$ setup time.

t_{OHEL} - Output enable to $\overline{CE}$ setup time.

t_{WHOL} - Output enable hold time after $\overline{WE}$ high.

t_{EHOL} - Output enable hold time after $\overline{CE}$ high.

t_{WLWH} - Write enable pulse width during write.

t_{WHWL2} - Minimum write enable high time.

t_{EHEL2} - Minimum chip enable high time after write.

t_{DVWH} - Data in setup time before $\overline{WE}$ high.

t_{DVEH} - Data in setup time before $\overline{CE}$ high.

t_{WHDX} - Data hold time after $\overline{WE}$ high.

t_{EHDX} - Data hold time after $\overline{CE}$ high.

t_{DVWL} - Minimum time from valid data out to next write.

t_{DVEL}	-	Minimum time from valid data out to next write.
t_{VDEHWL}	-	V_{OE} setup time to $\overline{WE}$ low (chip erase).
t_{WHVOEL}	-	V_{OE} hold time after $\overline{WE}$ high (chip erase).
t_{WLWL}	-	Cycle time during chip erase operation.
t_{DVWL}	-	Data to $\overline{WE}$ setup time (chip erase).
t_{ELWL}	-	$\overline{CE}$ setup time (chip erase).
t_{OVHWL}	-	Output setup time (chip erase).
t_{WHOH}	-	$\overline{OE}$ hold time (chip erase).
t_{OHEL}	-	Erase recovery (chip erase).
t_{DHWL}	-	Data setup time.
t_{WHDX}	-	Data hold time.

6.4.1 Timing parameter abbreviations. All timing abbreviations use lower case character with upper case character subscripts. The initial character is always t and is followed by four descriptors. These characters specify two signal points arranged by from-to sequence that define a timing interval. The two descriptors for each signal specify the signal name and the signal transition. (Note: There are exceptions for undefined signals.)

```
                                                   t   X    X    X    X
Signal name from which interval is defined ____________|    |    |    |
Transition direction for first signal ______________________|    |    |
Signal name to which interval is defined ________________________|    |
Transition direction for second signal ________________________________|
```

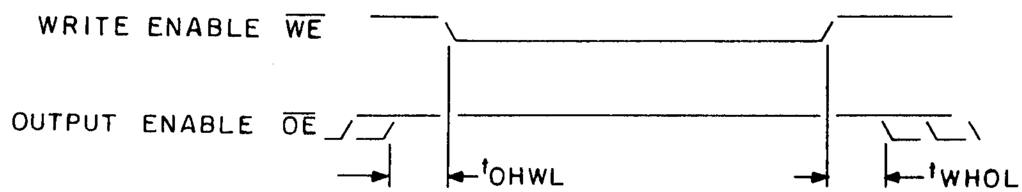
a. Signal definitions:

A = Address
W = Write enable
P = V_{CC}
D = Data in
E = Chip enable
R = Ready/busy
Q = Data out
O = Output enable

b. Transition definitions:

H = Transition to high
V = Transition to valid
Z = Transition to high impedance
L = Transition to low
X = Transition to invalid

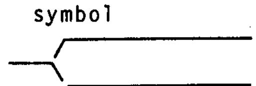
EXAMPLE:



The example shows $\overline{OE}$ to $\overline{WE}$ setup time defined as t_{OHWL} and $\overline{OE}$ hold time after $\overline{WE}$ high defined as t_{WHOL}.

c. Timing limits: The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus address setup time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus the access time is shown as a maximum since the device will never provide data later than that time (even though most devices will supply data much sooner).

d. Waveforms:

Waveform symbol	Input	Output
	Must be valid	Will be valid
XXXXXXXXXXXXXXXX	Change from low to high	Will change from low to high
\\\\\\\\\\\\\\\\	Change from high to low	Will change from high to low
////////////////	Do not care: Any change permitted	Changing state unknown
---------------	Not applicable	Change to high impedance

6.5 Logistic support. Lead materials and finishes (see 3.3) are interchangeable. Unless otherwise specified, microcircuits acquired for Government logistic support will be acquired to device class B (see 1.2.2), and lead material and finish C (see 3.3). Longer length and lead forming shall not affect the part number.

6.6 Handling. MOS devices shall be handled with certain precautions to avoid damage due to accumulation of static charge. Input protective devices have been designed in the chip to minimize the effect of this static buildup. However, the following handling practices are recommended:

a. Devices should be handled on benches with conductive and grounded surface.

b. Ground test equipment and tools.

c. Handling of devices by the leads should be avoided.

d. Store devices in conductive foam or carriers.

e. The use of plastic, rubber, or silk in the MOS area should be avoided.

f. Relative humidity should be maintained above 50 percent, if practical.

g. Operator should be grounded when handling devices.

6.7 Testing by inference. Testing by inference is the validation of the performance of a parameter by measurement of the correct performance of a dependent parameter or function.

Slash sheet number	Generic part number
/260-01-BXX	28C64-350
/260-01-BYX	28C64-350
/260-01-BZX	28C64-350
/260-02-BXX	28C64-300
/260-02-BYX	28C64-300
/260-02-BZX	28C64-300
/260-03-BXX	28C64-250
/260-03-BYX	28C64-250
/260-03-BZX	28C64-250
/260-04-BXX	28C64-200
/260-04-BYX	28C64-200
/260-04-BZX	28C64-200
/260-05-BXX	55C64-250
/260-05-BYX	55C64-250
/260-05-BZX	55C64-250
/260-06-BXX	28C65-250
/260-06-BYX	28C65-250
/260-06-BZX	28C65-250
/260-07-BXX	28C65-350
/260-07-BYX	28C65-350
/260-07-BZX	28C65-350

CONCLUDING MATERIAL

Custodians:
Army - ER
Navy - EC
Air Force - 17
NASA - NA

Review activities:
Army - AR, MI
Navy - OS, SH, TD
Air Force - 11, 19, 85, 99
DLA - ES

User activities:
Army - SM
Navy - AS, CG, MC

Preparing activity:
Air Force - 17

Agent:
DLA - ES

(Project 5962-1147)